REMARKS/ARGUMENTS

Claims 1-81 were originally filed in this application.

Claim 1-24 are allowed.

Claims 25-65 were withdrawn as a result of an earlier restriction requirement. Applicant reserves the right to file one or more continuation or divisional application(s) related to subject matter of these claims.

Claim 66 has been cancelled.

Claim 67 is amended.

Claims 68-69 have been cancelled.

Claims 70-81 were withdrawn as a result of an earlier restriction requirement.

New claims 82-85 have been added.

Accordingly, claims 1-24, 67, and 82-85 remain in this application.

The Rejection of Claims 66 – 69 Under 35 U.S.C. 102(b):

Claims 66 – 69 were rejected under 35 U.S.C. 102(b) as being anticipated by Shekar, et al. (U.S. Patent 5,294,816 – hereinafter "Shekar"), of which claims 66, 68, 69 have been canceled, rendering their rejection now moot.

Claim 67 of the present application, as now amended, recites a thyristor semiconductor memory device with a transistor serving as a current shunt to shunt low-level leakage current of at least one of the two base regions of the thyristor. The other of the two base region is electrically coupled to a gate of the transistor. Applicants submit that this inventive structure for a thyristor in a memory cell is distinguishable from Shekar, and further that one of ordinary skill in the art would find no disclosure nor

suggestion from the teachings of Shekar leading to the features of the present invention as recited in claim 67.

Shekar appears to teach of a high current MOS controlled thyristor switching device with a P-channel MOSFET ("PMOS") selectively operable to shunt current from a P-base region to a cathode contact of the high current switching thyristor. Shekar further discloses that the PMOS is selectively activated by application of a negative bias to the gate electrode that is capacitively coupled to the N-base region via an insulating layer on a semiconductor surface (column 6, lines 54-62). A careful reading of Shekar reveals that the gate electrode of the PMOS is independently biased, most likely by switching control circuitry outside the thyristor as would be understood by a person skilled in the art. Accordingly, it is submitted that Shekar does not explicitly nor implicitly teach or suggest biasing the gate from a region of the thyristor, let alone coupling the gate electrode of the transistor to one of the two base regions of the thyristor. Indeed, applicants further submit that the equivalent circuit of FIG. 3 of Shekar seems to expressly corroborate this view, especially when taken together with other teachings of Shekar.

Shekar Teaches Away From Claimed Invention:

Applicants respectfully note that the gate terminal shown for the equivalent circuit, as represented in FIG. 3 and as taught by Shekar, has been left as a separate stand-alone terminal (G). Further, Shekar teaches that "once the thyristor is turned-on, current flow can be shut off by application of a negative bias" (column 3, lines 12-14). Accordingly, applicants submit that not only do Shekar's teachings differ from the features of the embodiment to the present invention as recited in claim 67; but, indeed, applicants further submit that these teachings of Shekar teach away from the features recited in claim 67. Shekar teaches modulation of the thyristor and application of a negative bias to assist turn-off of the high current thyristor switching device, via the diverting means (column 2, line 60 to column 4, line 6; see also, column 5, lines 13-27 and column 6, lines 57-62).

Different Fields and Purposes:

Additionally, and alternatively, applicants submit that one of ordinary skill in the art of semiconductor memory devices would not necessarily look to the field of high current switching devices such as the teachings of Shekar for obtaining ideas to improve the field of semiconductor memory devices. And, even if so examined, applicants further submit that the purposes of Shekar -- i.e., to obtain an ability to turn-off a high power current switching thyristor absent parasitic latch-up (column 5, lines 29-33) -- differ significantly from the majority of considerations associated with low power semiconductor memory devices, and so much so as to lead an artisan in the field of semiconductor memory devices away from serious study of Shekar. Finally, as submitted earlier herein and alternatively, even should such artisan closely study Shekar, applicants submit that the teaching of Shekar do not suggest of a thyristor semiconductor memory device with a low-level transistor shunt as presently recited in claim 67, and, indeed, would seem to teach of keeping the control terminal separate and isolated in order to be operable to allow selective modulation, selective application of a negative bias, and selective control by, e.g., a switch control means operable for selectively turning-off the switching thyristor -- i.e., teaching away from the features of the embodiment of the present invention as recited in claim 67.

No Motivation in Shekar Toward Embodiment of the Present Invention:

Applicants further respectfully submit that a person of ordinary skill in the art, upon reading Shekar, would not find any motivation for producing the semiconductor memory device as recited in claim 67 for applicants' claimed structure. In particular, the coupling of the gate of a MOSFET to a base region of a thyristor would seem to be against the logical flow from the essence of Shekar. The techniques of Shekar teach the art of a gating means and a diverting means used to assist control of switching (e.g., turn-off) of an emitter switching thyristor. The gating means and diverting means of Shekar's

teachings are enabled or disabled by switching the bias of the gate. As Shekar discloses, the diverting means is selectively enabled to turn-off the thyristor -- e.g., when the PMOS is activated by a negative gate bias, and the low resistivity P^+ diverter region is electrically connected to the cathode of the thyristor to shunt holes in the P-base region to the cathode via the diverter region thereof (column 5, lines 9-24).

According to the Shekar patent, the turn-off capability is made available by the selective application of the bias to the P-MOS device. It also is applicable to a parasitic thyristor formed in the structure for the main thyristor (column 5, lines 28-40). As understood by one skilled in the art, the gate polarity is switched for this type of high current switching operation by applying a bias voltage to the gate, which operability would not be available if one of the base regions of the thyristor were electrically connected to the gate.

Moreover, applicants set out to solve the problems related to maintaining a holding current sufficiently low to ensure acceptable standby current in memory cells and to reduce the sensitivity of the thyristor to various adverse conditions when in the blocking state. In contrast, Shekar is concerned with a problem of sustained latch-up mode of operation of a parasitic thyristor in high current application. In that regard, the shunting of hole current to the cathode of the Shekar thyristor(s) causes an increase in the holding current level to above its operation current that is typically in the range of 1 to 2.5 amperes (column 4, lines 37-41). The holding current of the Shekar thyristor(s) may be unlikely affected by a low-level leakage current in a base region, the magnitude of which may be substantially below one ampere. For a problem not anticipated by Shekar, applicants submit that it would not be logical to one of ordinary skill in the art, upon reading Shekar, to be motivated to identifying a problem being addressed by the disclosure of the present invention, let alone finding a solution to the problem per embodiments of the present invention.

In view of the above, applicants respectfully submit that the claimed inventive structure for a thyristor-based memory as recited in claim 67 is patentable over Shekar.

Likewise, it follows that new dependent claims 84 and 85 also are patentable at least for reason of depending upon patentable base claim 67.

Allowability of New Claims 82 and 83:

New dependent claims 82 and 83 have been added to recite features to some particular embodiments of the present invention as disclosed explicitly and/or implicitly in the original claims and/or disclosure (see, e.g., paragraph [0095]). Because these claims (82 and 83) depend upon an allowable base claim 2, applicants submit that they are also allowable at least for reason of being dependent upon an allowable base claim and also independently thereof because of their own respective features.

Applicants respectfully request that a timely Notice of Allowance be issued in this case. If a discussion with the Examiner would be helpful, applicants encourage the Examiner to contact the undersigned directly at 360-750-9936.

Respectfully submitted,

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